IN THE CLAIMS:

1. (Cancelled)

2. (Cancelled

3. (Cancelled)

4. (Cancelled)

5. (Cancelled)

6. (Cancelled)

7. (Cancelled)

8. (Cancelled)

9. (Original) A semiconductor device comprising:
a main die area containing functional circuitry:
a scribe line monitor area circumferentially surrounding the main die area; and
stress relief elements in the scribe line monitor area,

10. (Original) The semiconductor device of claim 9, wherein the stress relief elements include dummy vias in the scribe line monitor area.

11. (Original) The semiconductor device of claim ~~10~~ 9, wherein the scribe line monitor area includes at least a first metal layer, a dielectric layer on the first metal layer, and a second metal layer on the first dielectric layer.

12. (Original) The semiconductor device of claim 11, wherein the dielectric layer is a low k dielectric layer.

13. (Original) The semiconductor device of claim 12, wherein the first and second metal layers contain non-functional metal tiles.

14. (Original) The semiconductor device of claim 13, wherein at least one of the dummy vias is connected between one of the metal tiles in the first metal layer and one of the metal tiles in the second metal layer.

15. (Original) The semiconductor device of claim 14, wherein the scribe line monitor area includes a saw lane, the dummy vias being located between the saw lane and the main die area.

16. (Currently amended) A semiconductor arrangement comprising:

a main die area;

a surrounding area circumferentially surrounding the main die area; and

crack stop elements in the surrounding area, **wherein the crack stop elements include dummy vias.**

17. (Cancelled)

18. (Currently amended) The semiconductor arrangement of claim **16** ~~17~~, wherein the surrounding area is a scribe line monitor area.

19. (Currently amended) **A semiconductor arrangement comprising:**

a main die area;

a surrounding area circumferentially surrounding the main die area; and

crack stop elements in the surrounding area, wherein the crack stop elements include dummy vias and the surrounding area is a scribe line monitor area that ~~The semiconductor arrangement of claim 18, wherein the scribe line monitor area~~ includes a first metal layer, a dielectric area on the dielectric layer, and a second metal layer on the dielectric layer, each of the first and second metal layers including non-functional metal tiles, and at least some of the dummy vias being connected between the metal tiles of the first and second metal layers.

20. (Original) The semiconductor arrangement of claim 19, wherein the dielectric layer comprises a low k dielectric material.